REMARKS

Claims 1-28 are pending in the application, with claims 1, 11, and 19 being the independent claims.

Applicant respectfully traverses the Examiner's rejection of each independent and dependent claim pending in the application.

Rejection under 35 U.S.C. § 101

Claims 1, 11 and 19 are rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. The Examiner states that the independent claims comprise a practical application, but do not produce tangible results such as manipulating memory, a display, or input/output.

Claims 1, 11, and 19 have been amended to further clarify the tangible results produced by the present claims. According to the technique of the present claims, an address is aligned such that, when the address is stored in memory in a K-bit word, the N least significant bits of the K-bit word will each be 0. Information is then encoded into N bits. These N bits are then stored in memory in the N least significant bits of the K-bit word, the same N bits that were 0 after the aligned address was stored in memory. The tangible result is the storage of information, comprising the information encoded into N-bits, in a memory, and specifically within the N least significant bits of a K-bit word that is already stored in memory, where the remaining K-N bits represent an address stored in memory.

By way of example, consider the storage in memory of an object header. For this example, the memory is configured such that each word is composed of 8 bits. The object header may contain an 8-bit address which points to another location in memory that contains information pertinent to the object's type. The object header may additionally contain 4-bits worth of information, pertinent to this specific instance of the object. The object header would normally need to be at least 12 bits in length, requiring 2 words, for a total of 16 bits, in this example's memory configuration. According to the present disclosure, it is possible to have this object header be only 1 word, for a total of 8 bits. The 8-bit address is aligned such that it's last 4 bits are 0's.

For example, an aligned 8-bit address may be 1101000. This is address is stored in memory in the object header in an 8-bit word. The additional 4-bits of information may then be encoded as 1001. These additional 4-bits of information may then be stored in memory in the 4 least significant bits of the 8-bit word in the object header in which the address 1101000 is already stored. Thus, the 8-bit word in the object header becomes 11011001. The claims, as amended, manipulate memory to produce a tangible result within that memory.

Rejections under 35 U.S.C. § 112

Claims 1, 11, and 19 are rejected under 35 U.S.C. 112 as failing to particularly point out and distinctly claim the subject matter which application regards as the invention. The Examiner asks what type of information is encoded by the claims of the present application, and what happens to this information after it is encoded.

The type of information encoded may be any type of information. Paragraph 33 of the present application discusses examples of the plurality of types of information that may be encoded. Examples of the types of information that may be encoded are information related to fast virtual method dispatching, thin-locking, generating effective hash codes, information related to garbage collection, information related to reflection. Any information that can be stored in a memory in N bits can be encoded.

The claims, as currently amended, clarify what happens to the information after is encoded. As discussed above, once the information is encoded it is stored in a memory within the N least significant bits of the K-bit word in which the aligned address is already stored. The subject matter of the present disclosure has been particularly pointed out and distinctly claimed.

Rejections under 35 U.S.C. § 102

Claims 1-18, 11-16, and 19-26 are rejected under 35 U.S.C. 102(e) as being anticipated by prior art.

Claims 1-18, 11-16 and 19-26 are rejected as being unpatentable over U.S. Patent No. 6,003,123 (hereinafter "Carter"). Applicant respectfully traverses the rejection.

With respect to independent claims 1, 11 and 19, the Carter does not contain each and every limitation present in the claims.

Carter does not teach the techniques of claims 1, 11 and 19 of aligning an address stored in a K-bit word such that the N least significant bits are zero and encoding information in the N least significant bits. Carter discloses a guarded pointer wherein an address is stored in two parts, as a 54-L bit segment part and an L-bit offset part. The pointer also contains 6 bits which specify a value for the L variable and 4 bits which contain information regarding permissions to perform operations with the pointer. (Carter, Fig. 1A, col. 4 lines 40-54). The word in which this guarded pointer is stored is a 64-bit word. (Carter, col. 4 lines 40-41). The address contained within the word is not aligned such that the N least significant bits are 0. The 54-L bit segment part and the L-bit offset part are combined as a single address which identifies a specific location in a virtual memory mapped space. In most instances at least one of the N least significant bits of this address will be non-0. For any positive N<54, there are some addresses which, when stored in the guarded pointer of Carter, will have their N least significant bits equal to 0. In these cases, no information will be encoded into the bits. Instead, the fact that the N least significant bits are equal to 0 is the information. This information is that the offset segment of the specified adddress consists of N 0's. It is not possible to encode any further information in the N least significant bits if they are all 0's. They must be left as 0's.

This is wholly different from the teaching of the present application, wherein the N least significant bits are used for the storage of non-address related information. The technique of the present application encodes information into the N least significant bits of a K-bit address by changing the bits from 0's to whatever value is necessary to represent the information being encoded. When an address is read, only the first K-N bits are considered to represent the actual address. Thus, for an N of 4 and a K of 8, an address of 10100000 may be stored as 10101100, but will be still be recognized as 10100000. Using the techniques disclosed in Carter, such a change would result in the address itself being changed from 10100000 to 10101100, as the N least significant bits would be considered part of the address. In the technique of the present application the N least significant bits are recognized as having been used to encode other, non-address information, such as, for instance, garbage collection data. This is accomplished by insuring that the object stored in memory which is pointed to by the address is stored such that the N least significant bits of its address are 0's in a process known as memory alignment.

Therefore, Carter does not disclose the techniques of claims 1, 11, and 19 of the present application of aligning an address stored in a K-bit word such that the N least significant bits are zero and encoding information in the N least significant bits, as Carter does not align an address such the N least significant bits are 0, and does not encode information in the N least significant bits of an address. Independent claims 1, 11 and 19 are allowable over Carter.

Claims 2-10, 12-18, and 20-28 depend from the independent claims which are allowable over Carter as discussed above.

Conclusion

All of the stated grounds of rejection have been properly traversed. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

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Respectfully submitted,

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Attachments